IN THE SPECIFICATION

Please amend the paragraph starting on page 3, line 7 as follows:

~~FIG. 2 is~~ FIGS. 2A and 2B are a detailed block diagram of a preferred embodiment of the circuit of FIG. 1;

Please amend the paragraph starting on page 3, line 11 as follows:

FIG. 4 is a block diagram of an alpha select circuit of the circuit of FIG. 1; ~~and~~

Please amend the paragraph starting on page 3, line 13 as follows:

FIG. 5 is a block diagram of a filter control circuit of the circuit of FIG. 1~~.~~; and

Please add the following paragraph starting on page 3, at line 15 as follows:

FIGS. 6A and 6B show a method illustrating a sequence of operations for each BME scan line.

Please amend the following paragraph starting on page 4, at line 15 as follows:

Referring to ~~FIG. 2~~ FIGS. 2A and 2B, a detailed block diagram of the data path circuit 102 and the filter control circuit 104 is shown. The data path circuit 102 generally comprises a

register 130, a multiplexer 132, a circuit 134, a circuit 136, and a circuit 138. The circuit 130 may be implemented as a register file. The register file 130 may comprise a number of register sets 131a-131n. The circuit 134 may be implemented as an alpha multiplier and accumulator (MAC) or a select circuit. The circuit 136 may be implemented as color component MACs. In one example, a circuit 136 may be implemented as a 3X color component MACs.

Please amend the following paragraph starting on page 18, at line 4 as follows:

Referring to ~~FIG. 6~~ FIGS. 6A and 6B, a method 200 illustrating a sequence of operations for each BME scan line is shown. At a state 202, the output counter 192 may be loaded with data from the signal FILTERSTART, and the pixel counter 190 (or the signal PIXCNT) may be set to 0. At a state 204, a single pixel of data may requested by the signal DATAREG. At a state 206, a shift is set active until all the register file 130 is full of the first data pixel. At a state 208, additional data may then be requested and shifted into the register file 130 normally. The pixel counter 190 (or the signal PIXCNT) may be incremented by 1 for each input pixel. At a state 210, data loading may stop when the signal PIXCNT equals the integer part of the signal OUTCNT. Therefore, an output calculation may start, triggered by the signal STARTCALC. At a state 212, the signals TAP and COEFADDR select the data and coefficient respectively for the first tap of the filter 100. The

signal ACC may be low to ensure MAC register 136 is cleared at the start of the calculation.